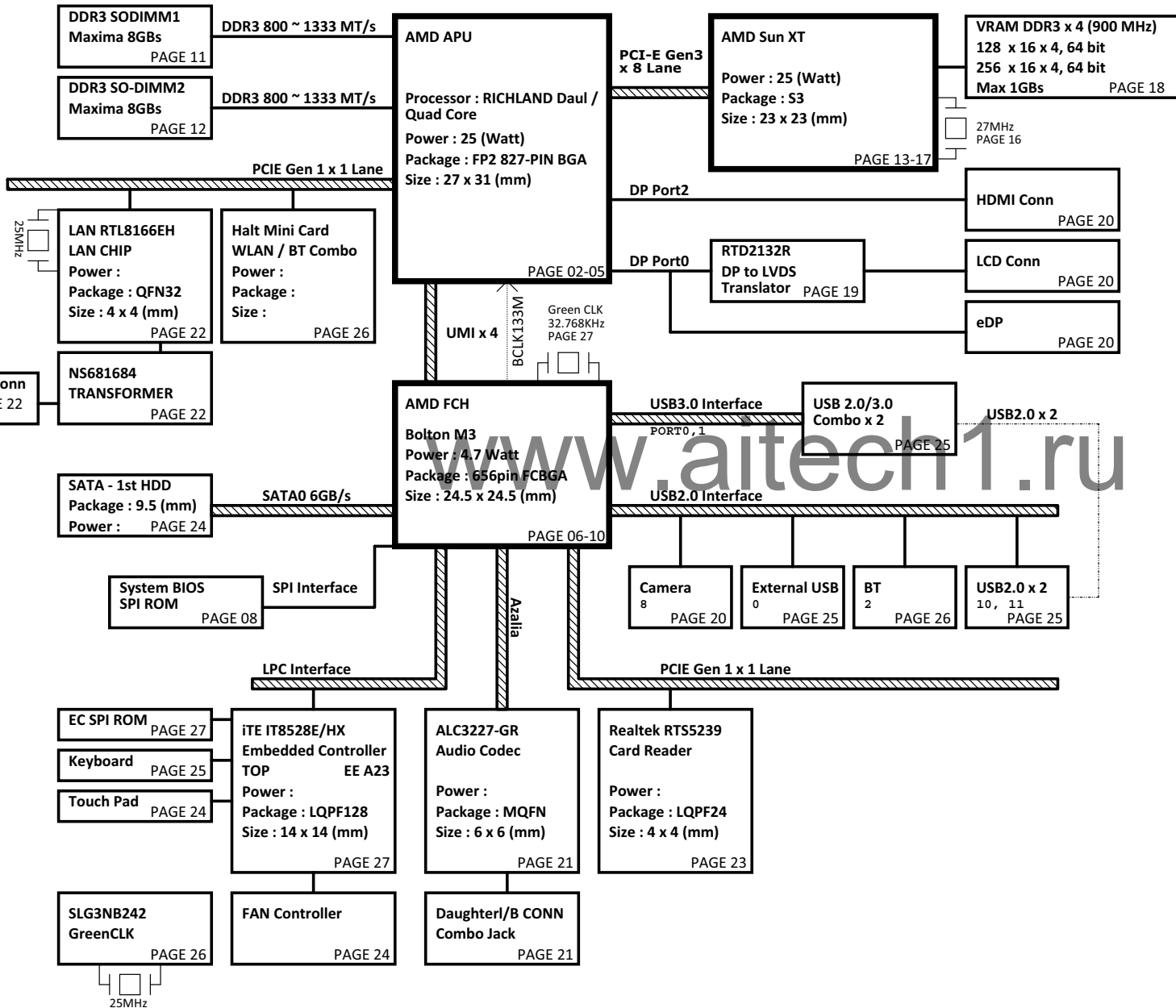


HAYAO_AMD RICHLAND DIS/UMA (14"/15.6") Ultra/Slim



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

BQ24728
System Charge Power (+BATCHG)

G5934RZ1U
System Discharge Power
(+1.5V/+3V/+5V)
(+3VSUS/+3VLANVCC/+1.1V)

Ricktek RT8223PZ
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

SL6277/RT8228AZ/AP3407A/ISL6208BCRZ
Processor Power (+VCC_CORE/
+1.2V/+2.5V/+VDDNB_CORE)

TP51216RUKR
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

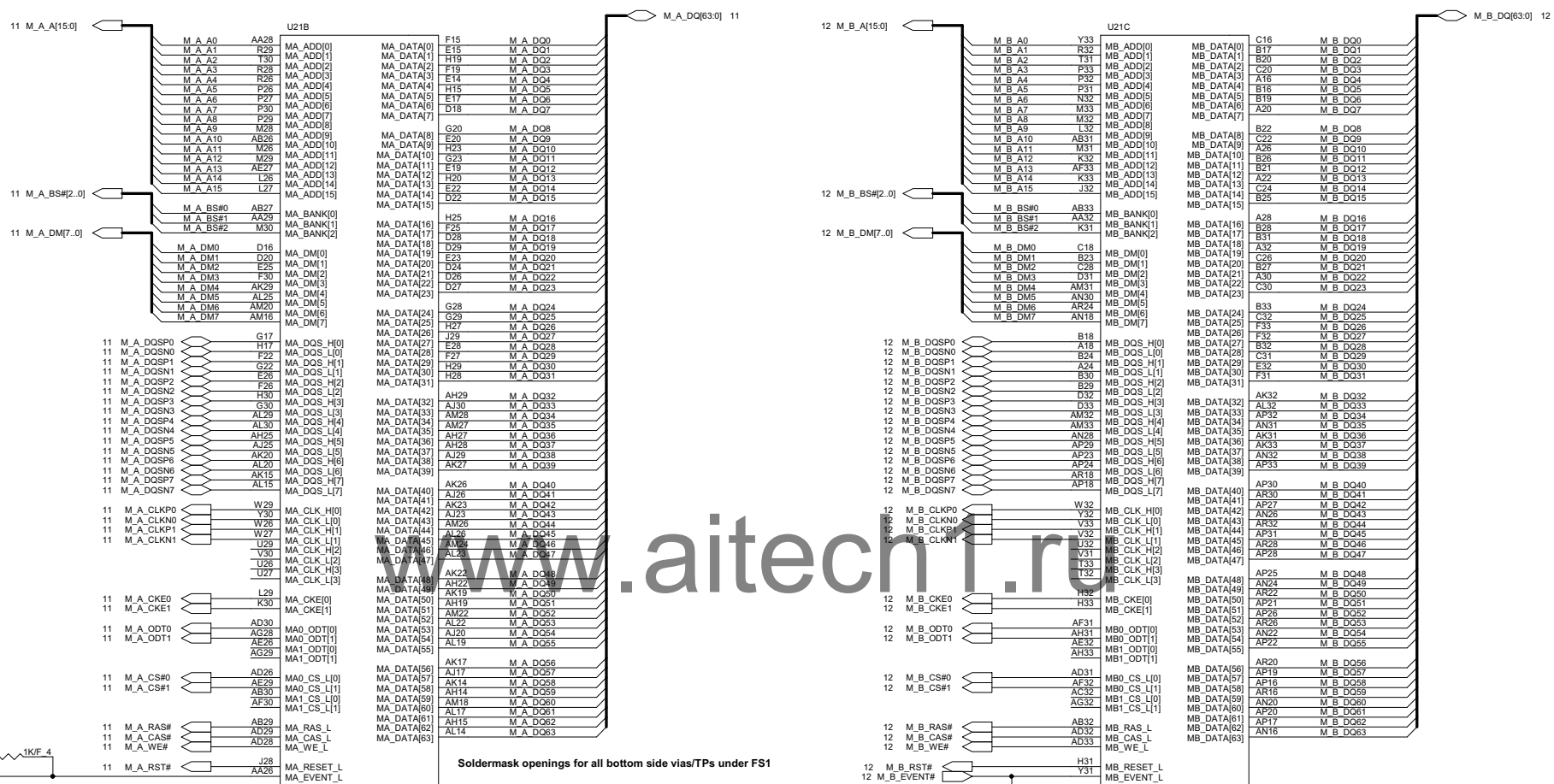
AOZ1237QI-02
PCH Power (+1.1VS5)

ADP3211A
DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/
+1.5V_VGA/+1.8V_VGA/+VDDCI)



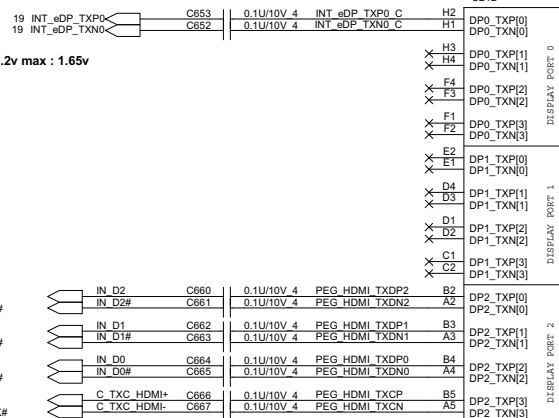
PROJECT : Richland FP2
Quanta Computer Inc.

Size A3	Document Number Block Diagram	Rev 1A
Date: Wednesday, May 08, 2013	Sheet	1 of 37



DP0 output to
eDP to LVDS converter

Display port power 1.5V min 1.2v max : 1.65v



4/19 HDMI change to DP2 for Comal.

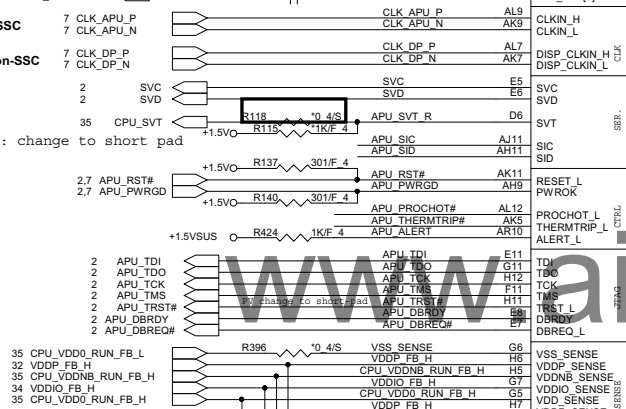
DP2 output to
HDMI connector

note --HDMI P&N can not swap

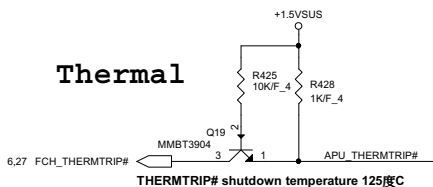
Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

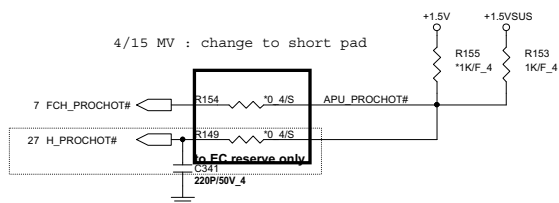
4/15 MV : change
to short pad



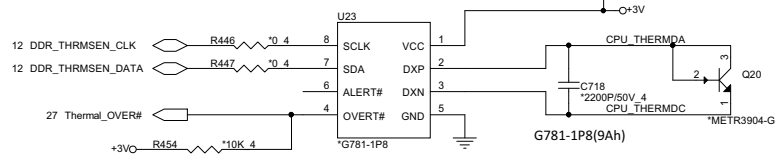
Thermal



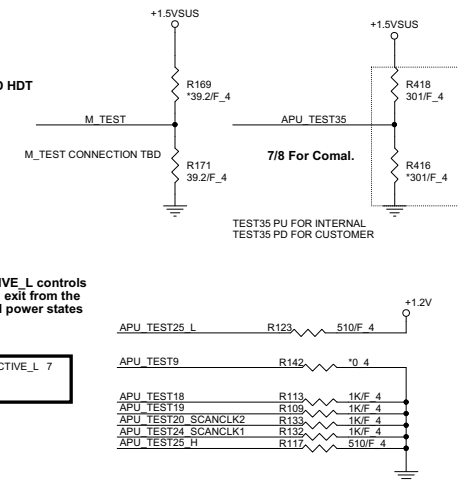
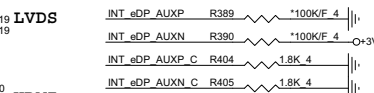
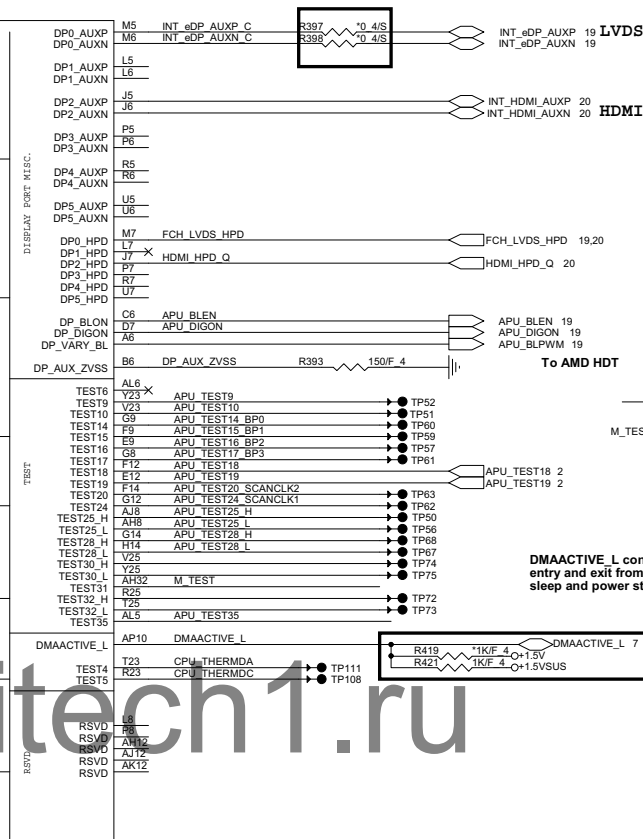
4/15 MV : change to short pad



Local Thermal Sensor

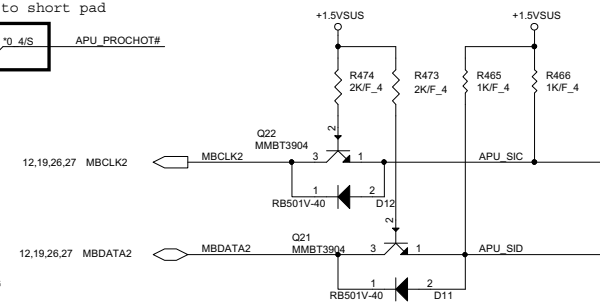
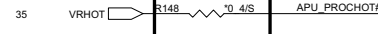


Place under CPU heat pipe



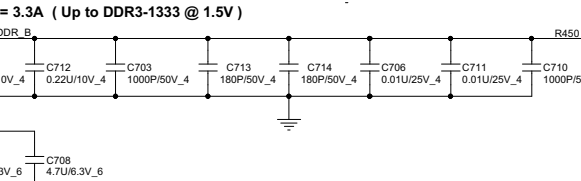
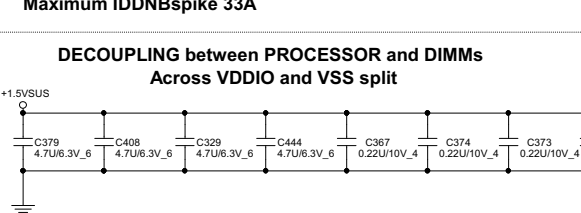
DMAACTIVE_L controls
entry and exit from the
sleep and power states

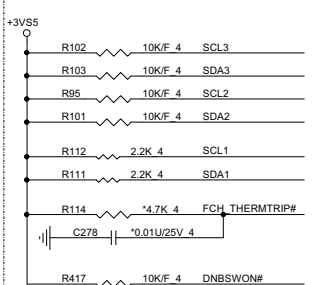
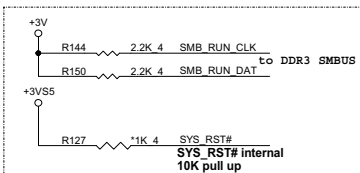
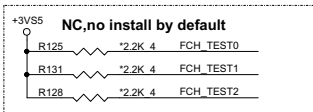
4/15 MV : change to short pad



PROJECT : Richland FP2
Quanta Computer Inc.

Size Document Number
Llano Display/Misc
Date: Wednesday, May 08, 2013 Sheet 4 of 37

PRINT-FAX-SERIES_BOASTS



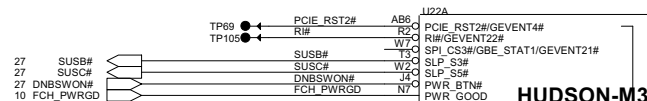
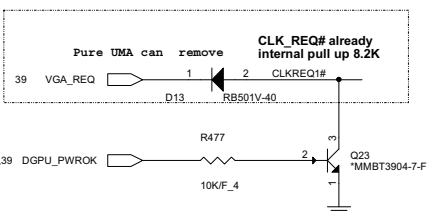
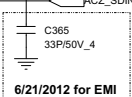
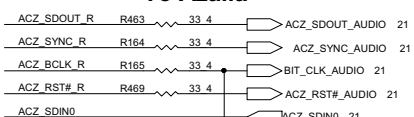
GEVENT0# internal pull Hi 8.2K to +3V
GEVENT1# internal pull Hi 8.2K to +3V
GEVENT23# internal pull Hi 8.2K to +3V
GEVENT5# internal pull Hi 8.2K to +3V55
PCI_E_WAKE# no need to pull
Hi resistor from check list

CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V

This pin is used to power down VGA DAC regulators when CRT no connected

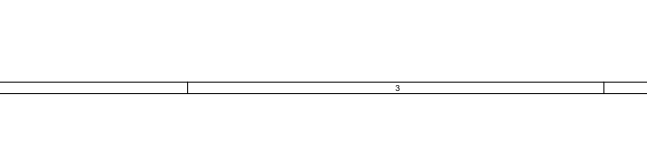
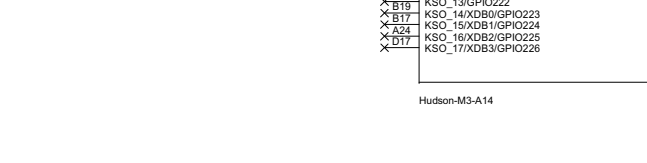
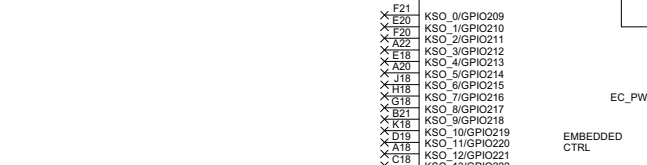
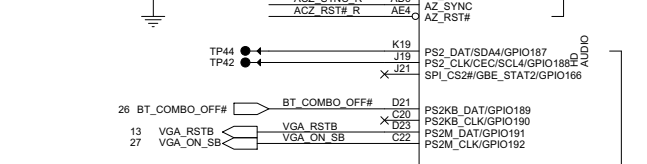
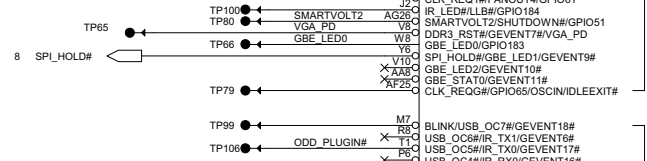
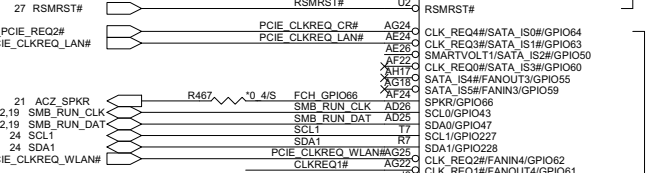
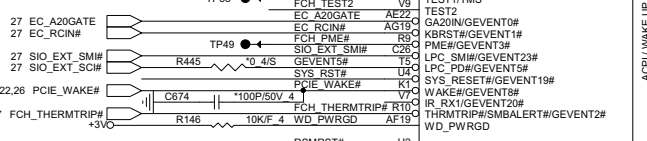
GEVENT16# internal pull Hi 8.2K to +3V55
GEVENT15# internal pull Hi 8.2K to +3V55

To Azalia

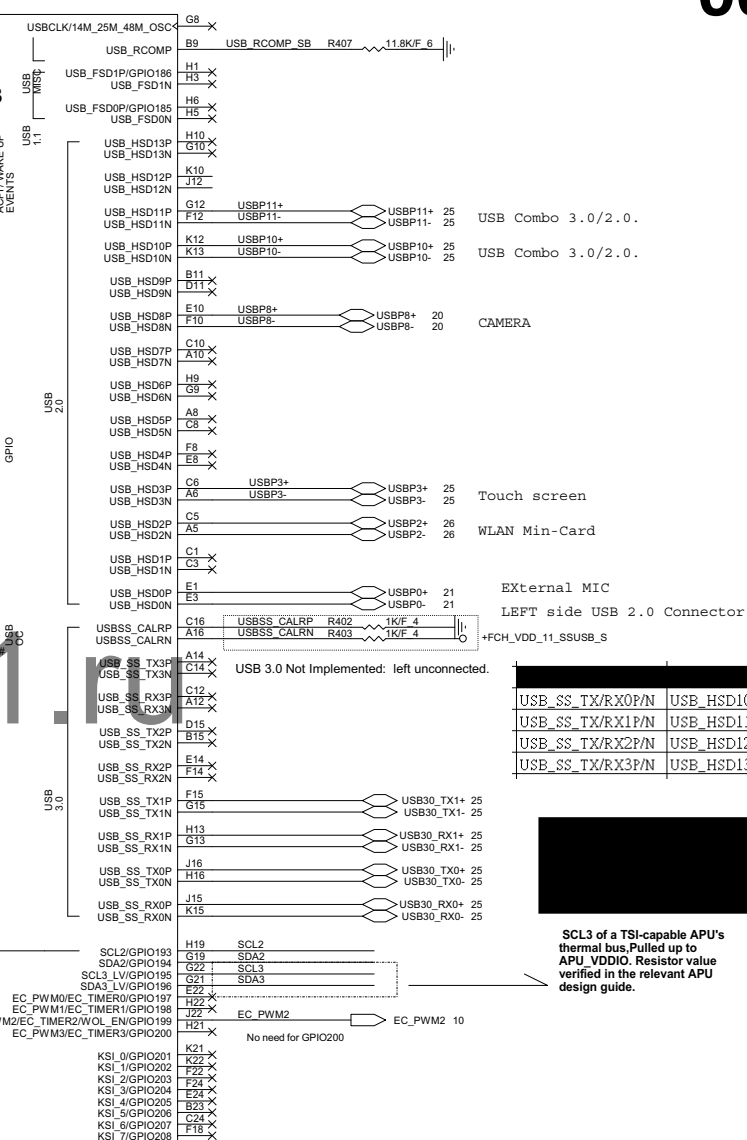


HUDSON-M3

Part 4 of 5



Hudson-M3-A14

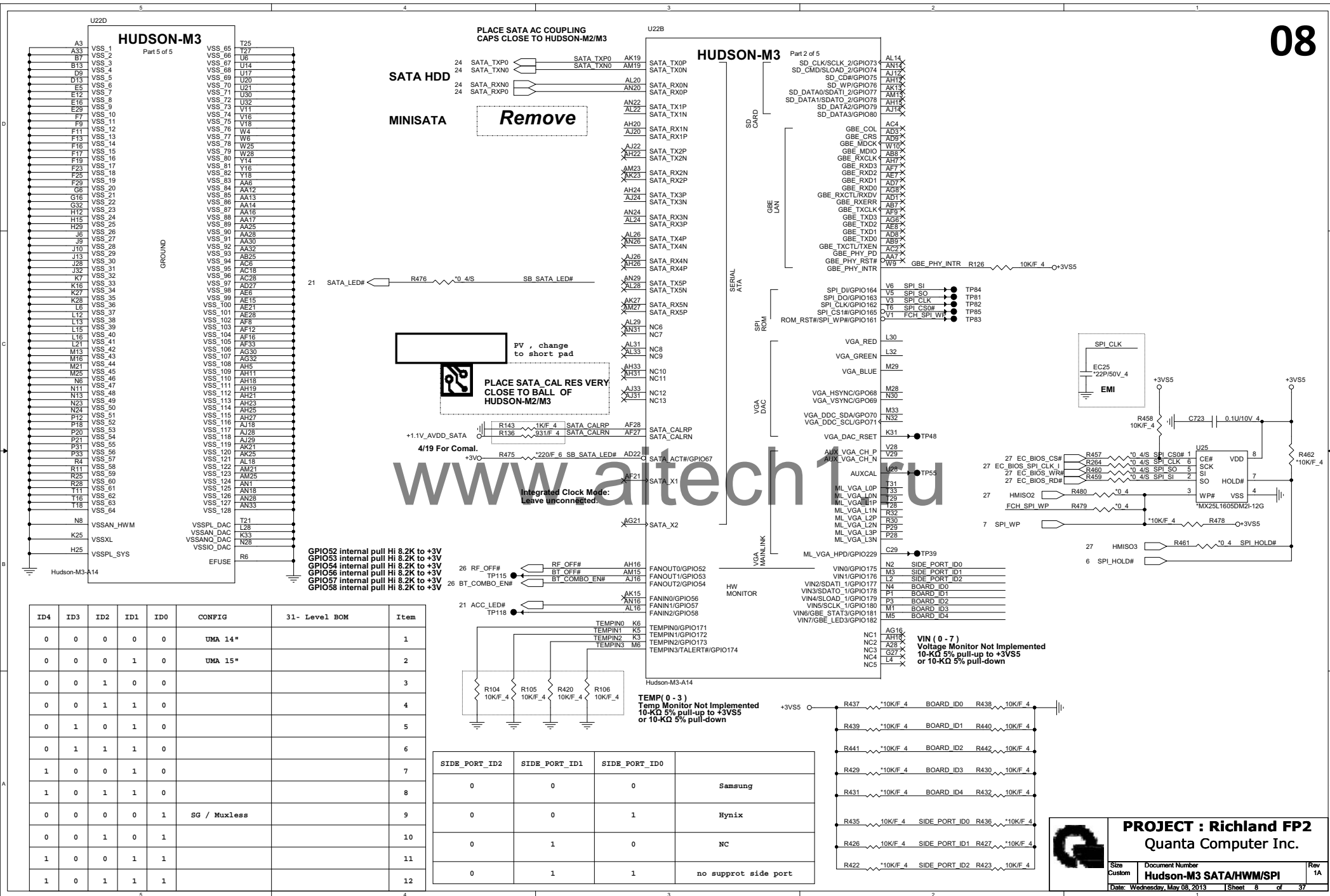


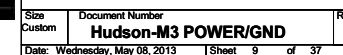
SCL3 of a TSI-capable APU's thermal bus. Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.



PROJECT : Richland FP2
Quanta Computer Inc.

Size Custom Document Number Hudson-M3 GPIO/USB/AZ/RGMI Rev 1A
Date: Wednesday, May 08, 2013 Sheet 6 of 37

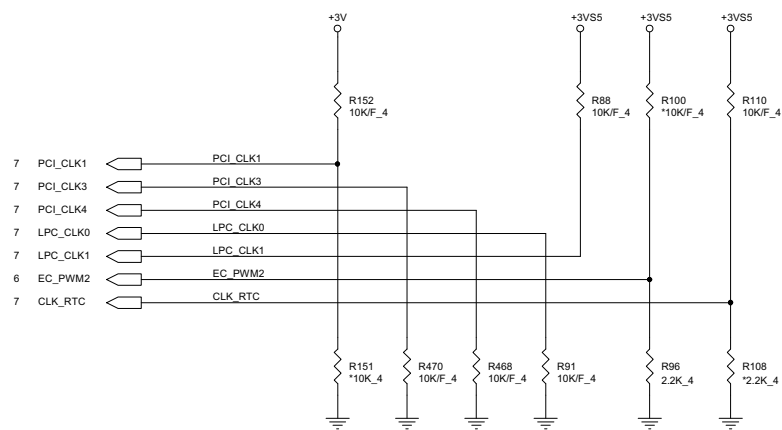




STRAPS PINS



OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

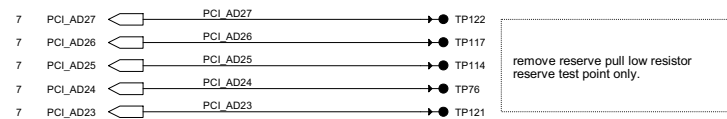


REQUIRED STRAPS

		PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	*****	ALLOW PCIe Gen2 DEFAULT	*****	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	LPC ROM	S5 PLUS MODE ENABLED DEFAULT
PULL LOW	*****	FORCE PCIe Gen1	*****	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	SPI ROM DEFAULT	S5 PLUS MODE DISABLED

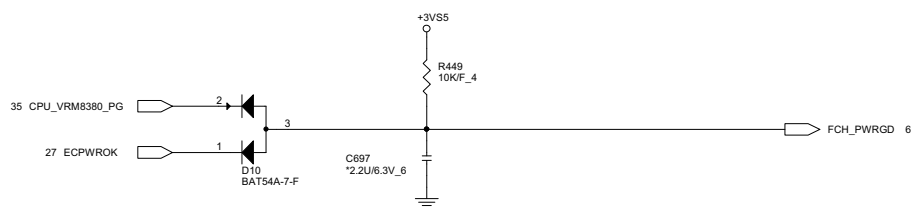
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



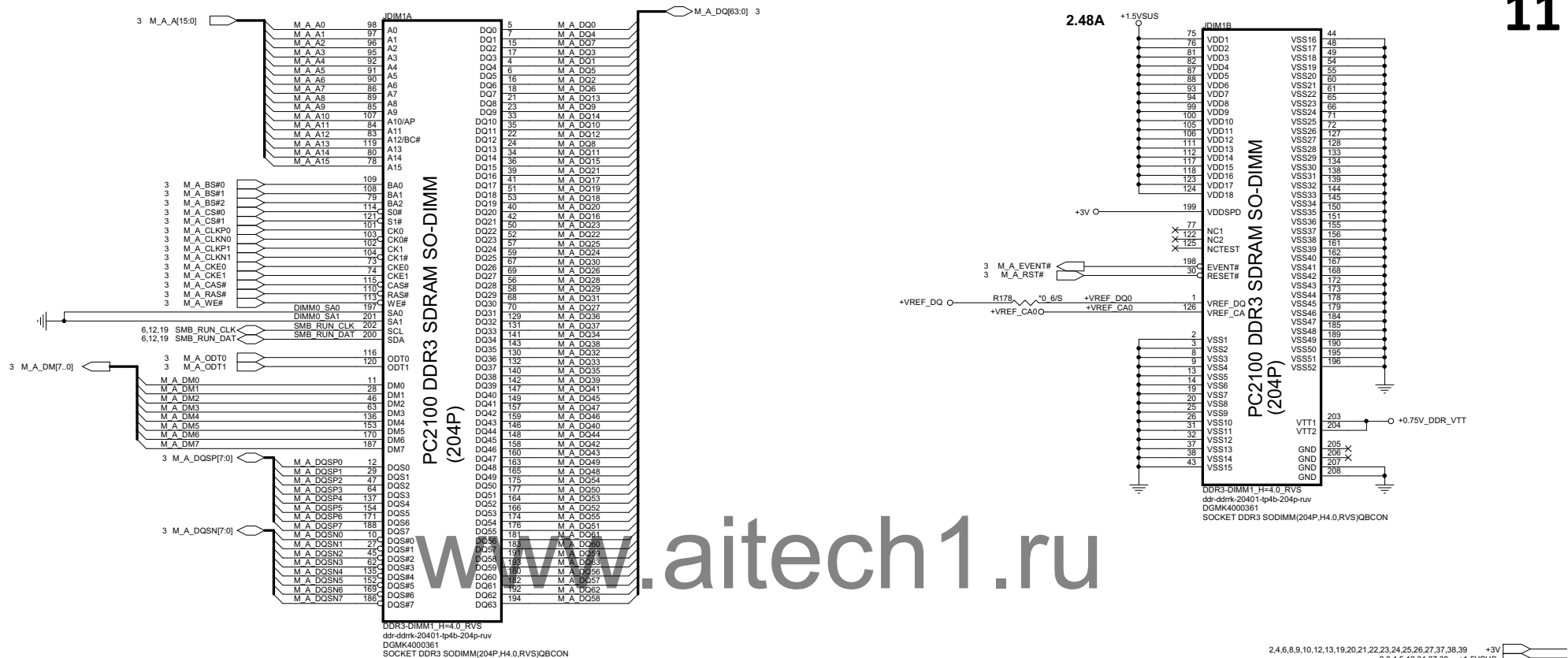
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD

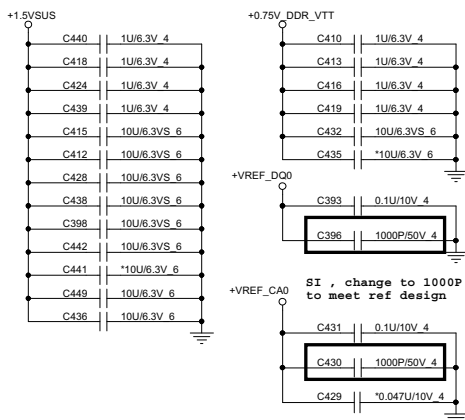


PROJECT : Richland FP2
Quanta Computer Inc.

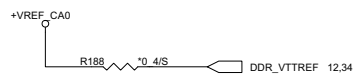
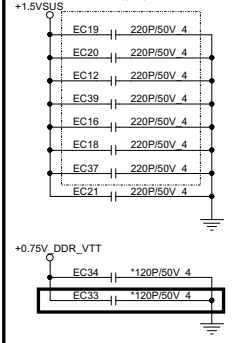
Size Custom	Document Number Hudson-M3 STRAP/PWRGD	Rev 1A
Date: Wednesday, May 08, 2013	Sheet 10 of 37	



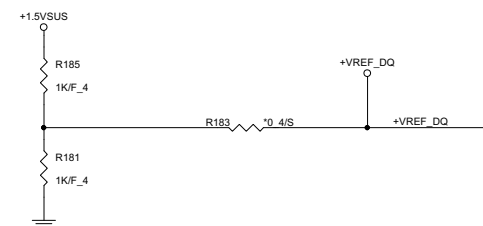
Place these Caps near So-Dimm0.



For EMI RESERVE
6/21/2012 for EMI

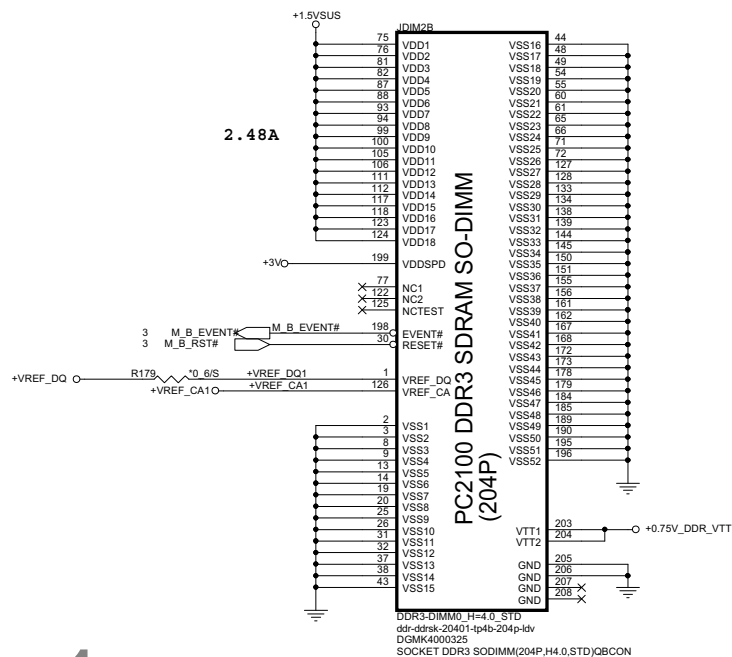


Reserved for AMD suggest



PROJECT : Richland FP2
Quanta Computer Inc.

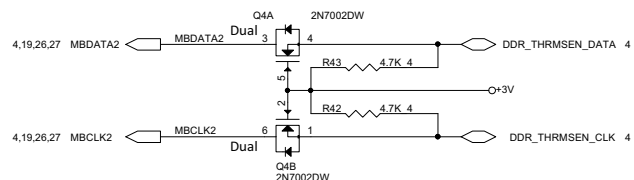
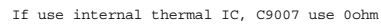
Size	Document Number	Rev
Custom	System Memory 1/2 (5.2H)	1A
Date: Wednesday, May 08, 2013	Sheet 11 of 37	



D052	188	M B D053
D053	174	M B D050
D054	176	M B D051
D055	181	M B D081
D056	193	M B D059
D057	191	M B D063
D058	193	M B D062
D059	190	M B D057
D060	192	M B D090

2,4,6,8,9,10,11,13,19,20,21,22,23,24,25,26,27,37,38,39 +3V
2,3,4,5,11,34,37,39 +1.5VSUS
11,34 +0.75V DDR VTT

Local Thermal Sensor

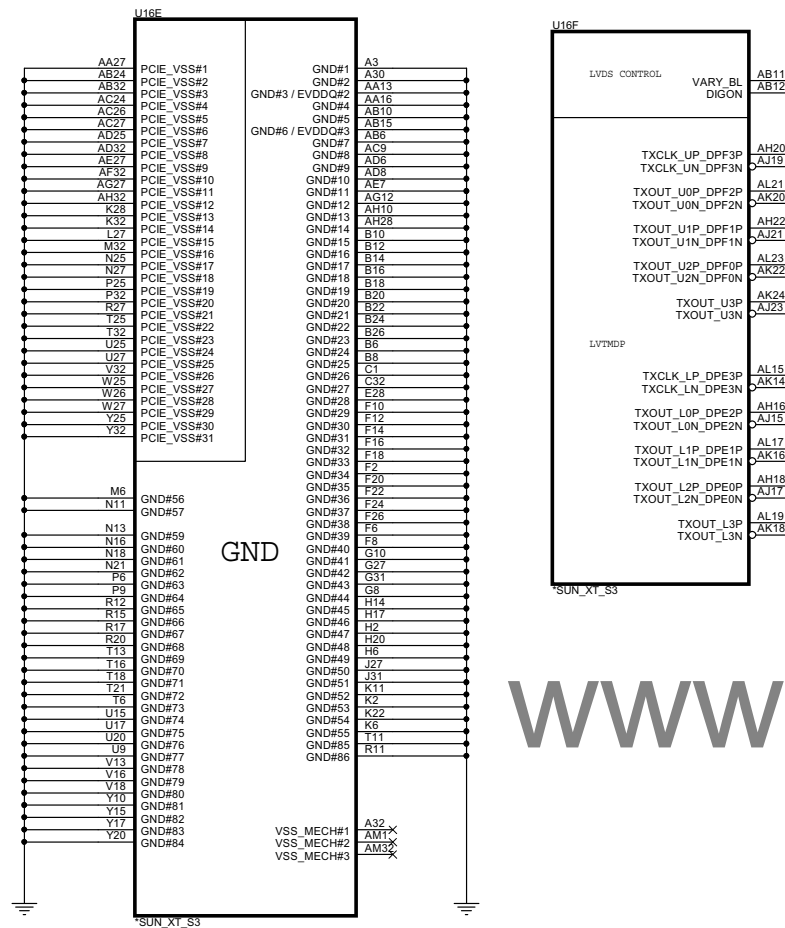


Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

PROJECT : Richland FP2
Quanta Computer Inc.



Size Custom	Document Number System Memory 2/2 (9.2H)	Rev 1A
Date: Wednesday, May 08, 2013	Sheet 12 of 37	



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

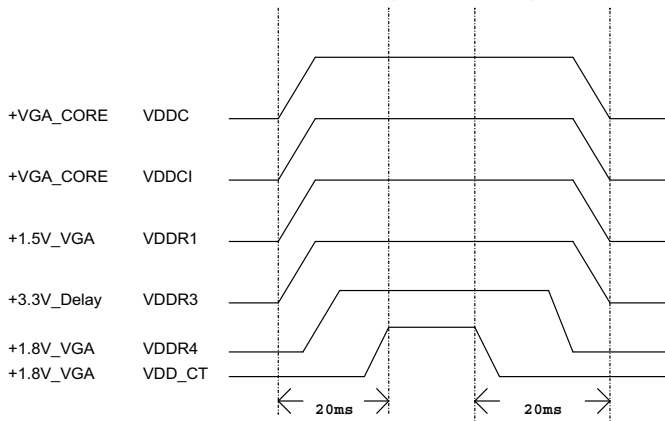
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPI00	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPI01	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPI02	RESERVED	0
RSVD	GPI08	RESERVED	0
BIF_VGA_DIS	GPI09	VGA ENABLED	0
RSVD	GPI021	RESERVED	0
BIOS_ROM_EN	GPI0_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPI0[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on SeymourWhistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSXNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPI021 H2SYNC GENERICC GPI08 GPI02

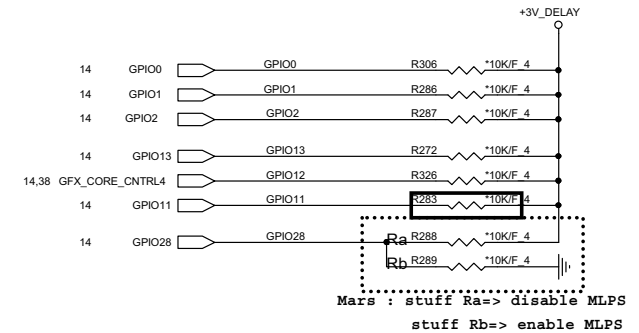
Power Up/Down Sequence



Memory Aperture size(Seymour)

GPI09 BIOSROM		GPI013 ROMIDCFG2	GPI012 ROMIDCFG1	GPI011 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

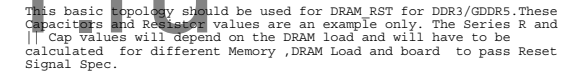


PROJECT :U73
Quanta Computer Inc.

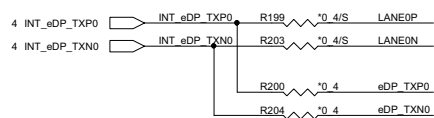
Size	Document Number	Rev
Custom	Sun S3 GND / LVDS/ Straps	1A
Date: Wednesday, May 08, 2013	Sheet 15 of 37	



Size Custom	Document Number Sun S3 Power_and_NC	Rev 1A
Date: Wednesday, May 08, 2013		Sheet 16 of 37





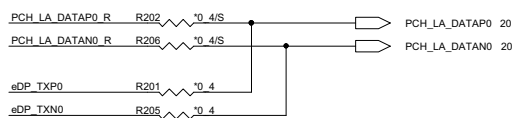


To LVDS Converter

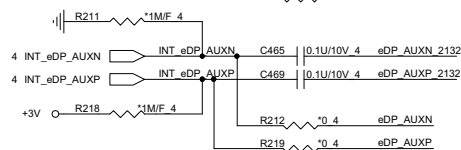
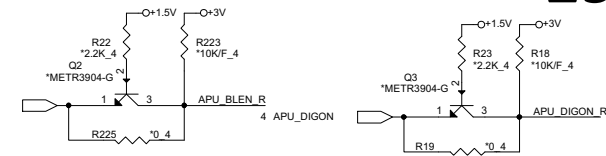
To eDP

From LVDS Converter

From APU



From APU

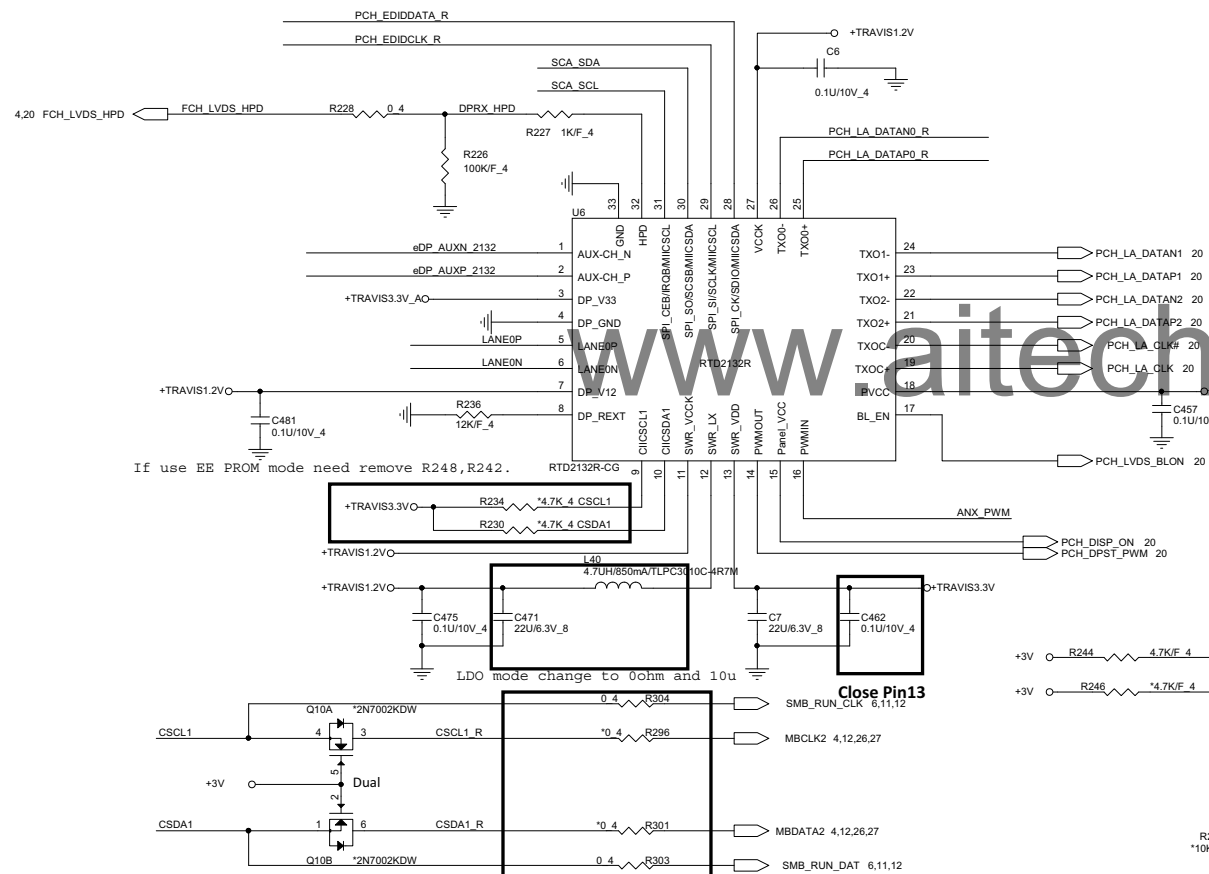
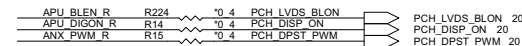
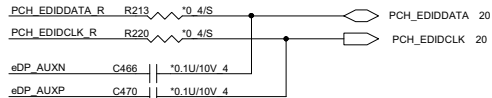


To LVDS Converter

To eDP

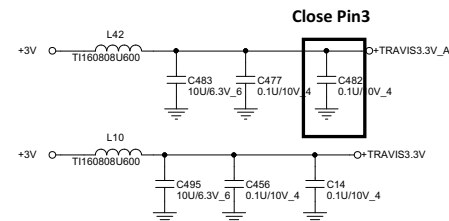
From LVDS Converter

From APU



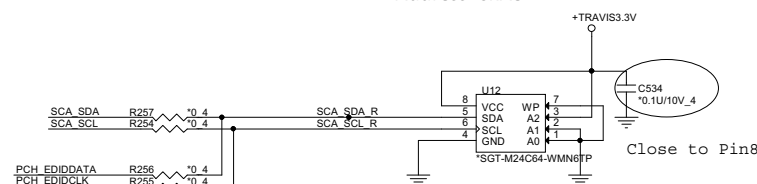
If use EE PROM mode need remove R248,R242.

EE PROM	R304,R308
EC OPTION	R307,R305



Close Pin3

Address=0xA8



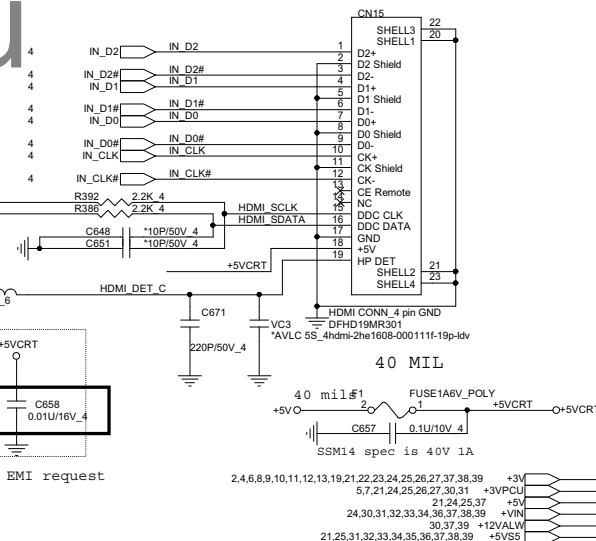
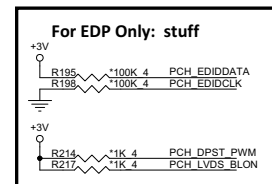
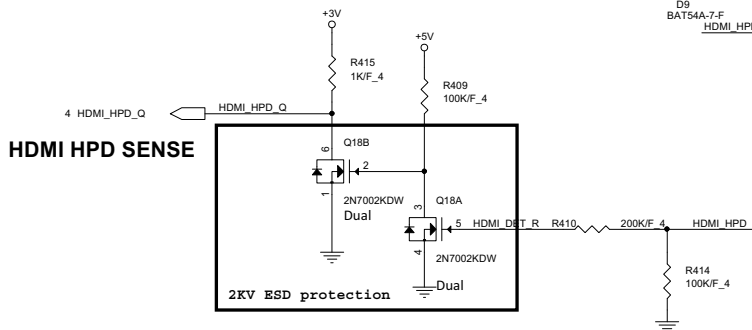
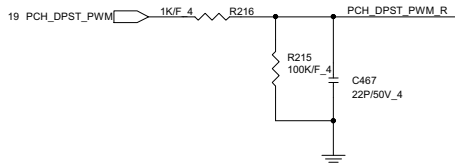
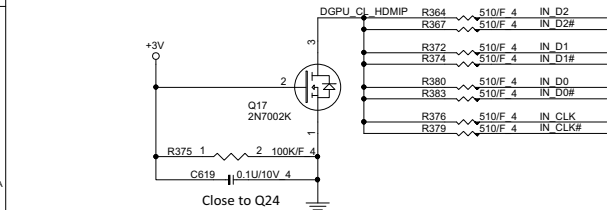
Close to Pin8

		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



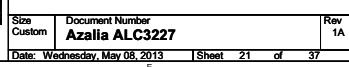
PROJECT : Richland FP2
Quanta Computer Inc.

Size Custom	Document Number RTD2132S	R
Date: Wednesday, May 08, 2013		Sheet 19 of 37

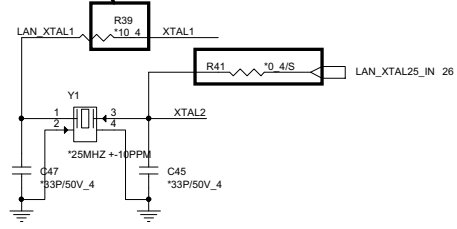
HDMI Conn.

PROJECT : Richland FP2
Quanta Computer Inc.

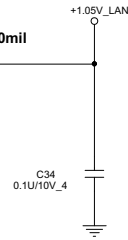
Size Custom	Document Number LCD Connector (LVDS)	Rev 1A
Date: Wednesday, May 08, 2013	Sheet 20 of 37	



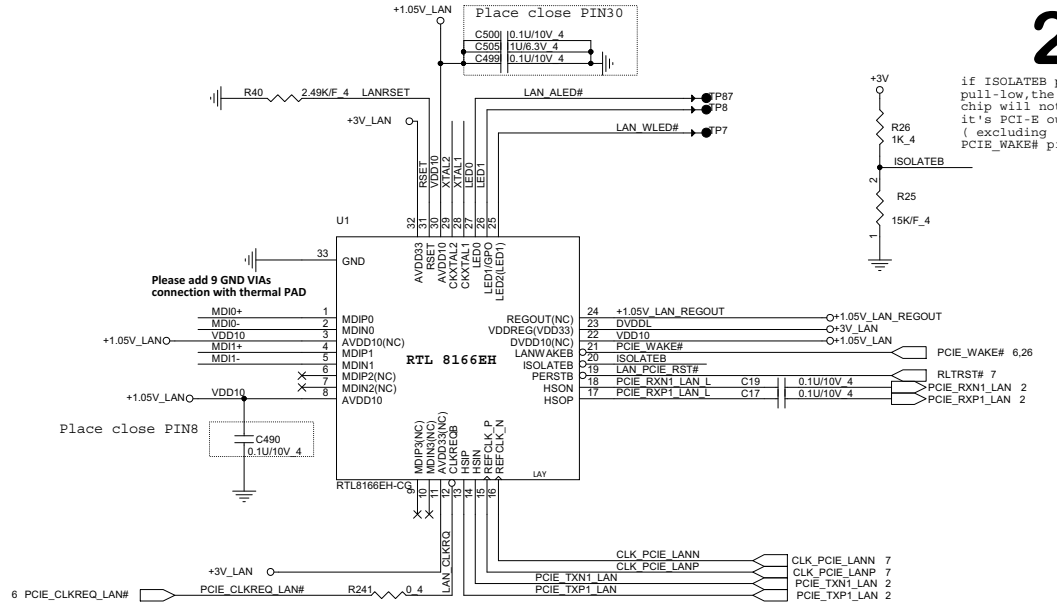
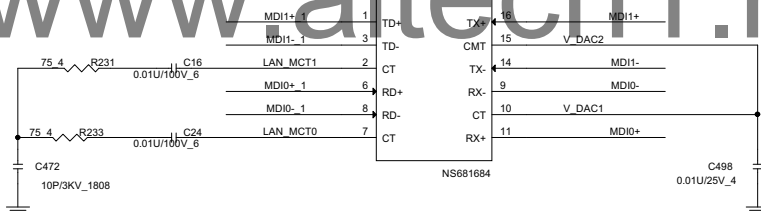
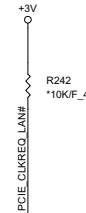
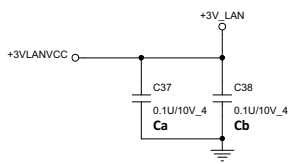
For EMI 0 ~ 22 ohm



>60mil Power trace Layout 宽度>60mil

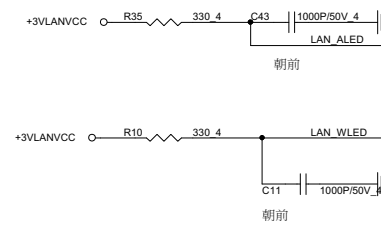
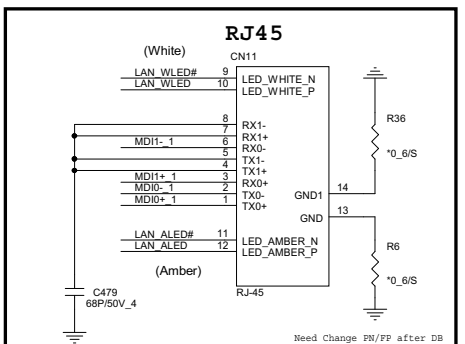


Place close PIN23 and PIN32



if ISOLATEB pin pull-low, the LAN chip will not drive its PCIE outputs (excluding PCIE_WAKE# pin)

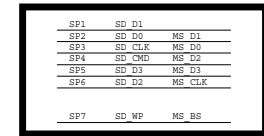
LAN conn



2,4,6,8,9,10,11,12,13,19,20,21,23,24,25,26,27,37,38,39 +3V 26,37 +3V_LANVCC

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Quanta Computer Inc.

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Reserve for EMI

SD D0	EC30	5.6P/16V 4
SD D1	EC29	5.6P/16V 4
SD D2	EC32	5.6P/16V 4
SD D3	EC31	5.6P/16V 4




Diagram showing the pin connections for CN14 (CARDREADER CONN DFHD11MR034) to the sdcad-cs1m-098-h-n-11p connector.

Pin	Signal
1	SD D2
2	SD D3
3	SD CMD
4	SD CD#
5	C/D
6	VSS1
7	VDD
8	SD_CLK
9	CLK
10	SD D0
11	SD D1
12	SD W/P
13	DAT1
14	W/P
15	GND

Additional connections shown:

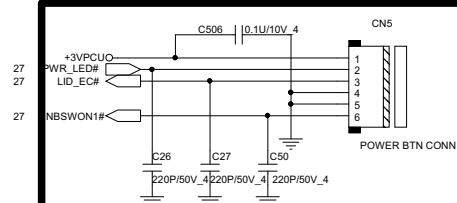
- +3V_CARD is connected to Pin 7 (VDD).
- Pin 15 is connected to GND.

Connector Labels:

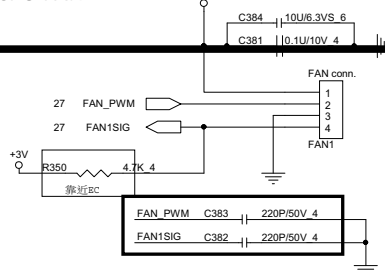
- CN14
- CARDREADER CONN DFHD11MR034
- sdcad-cs1m-098-h-n-11p

Power Button Connector

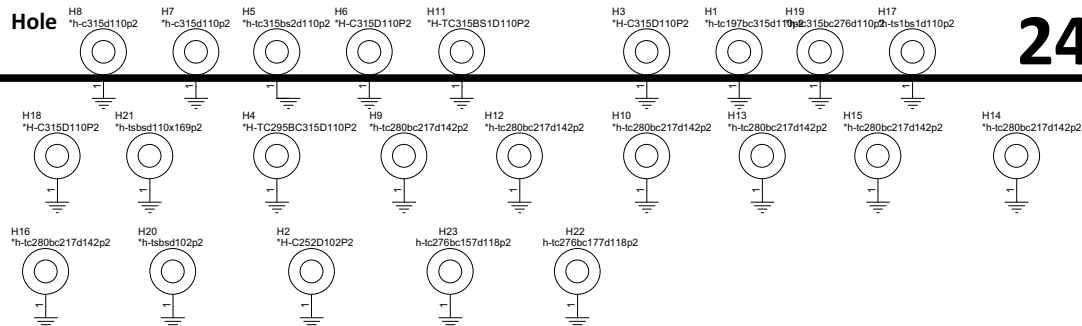
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



CPU FAN

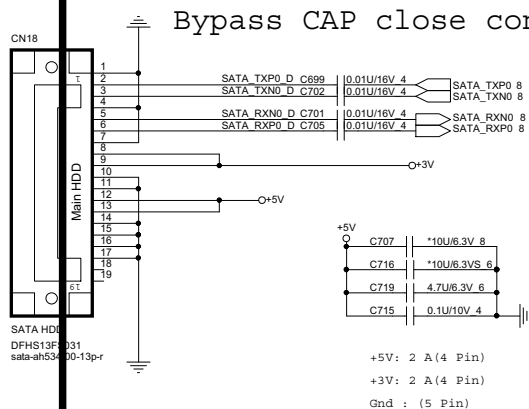


Hole

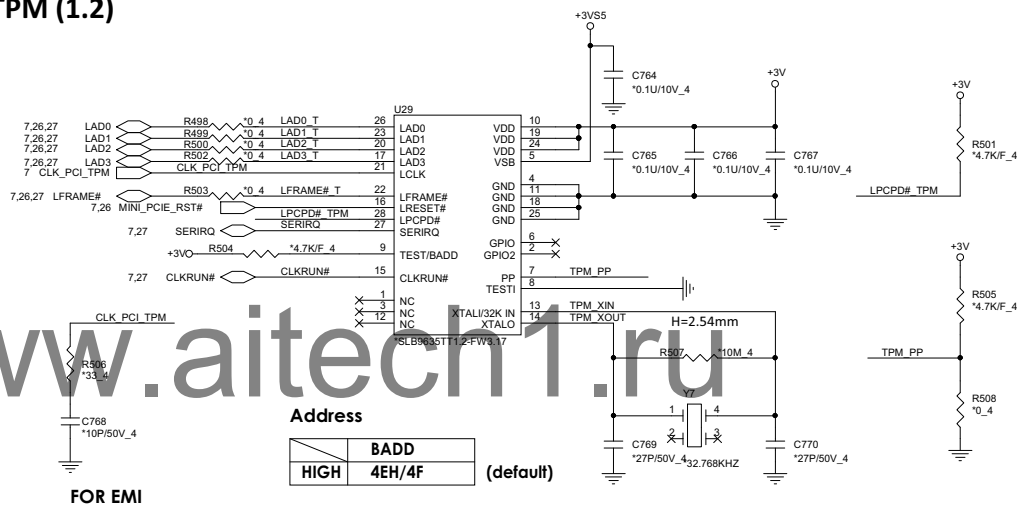


SATA HDD Connector(Cable type)

Bypass CAP close conn



TPM (1.2)

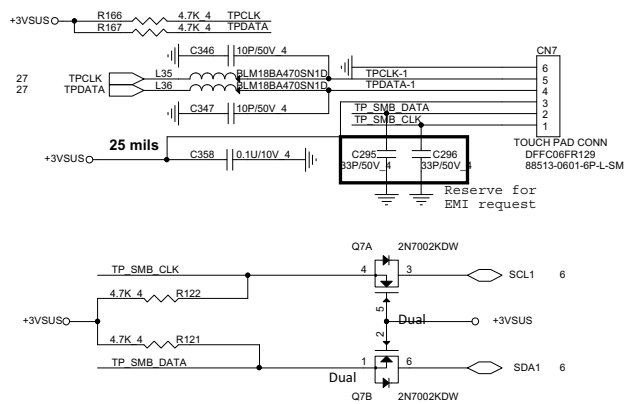
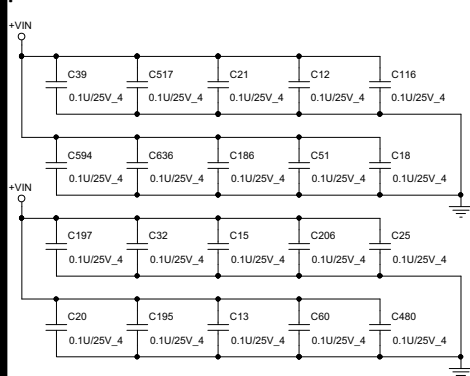


Address

	BADD
HIGH	4EH/4F (default)

FOR EMI

+VIN Cap

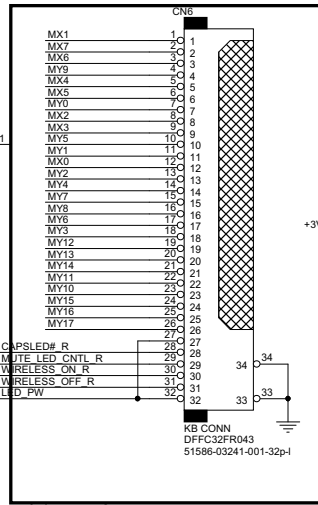
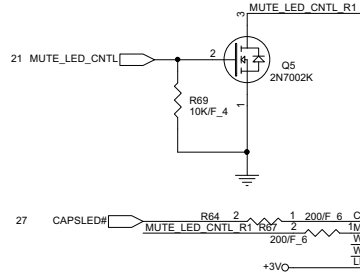


PROJECT : Richland FP2
Quanta Computer Inc.

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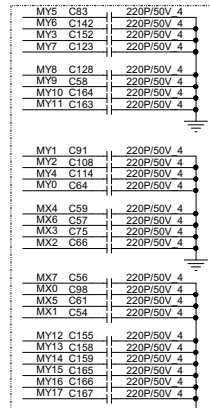
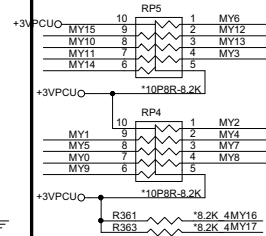
KEYBOARD Con.

27 MY[0..17] MY[0..17]
27 MX[0..7] MX[0..7]

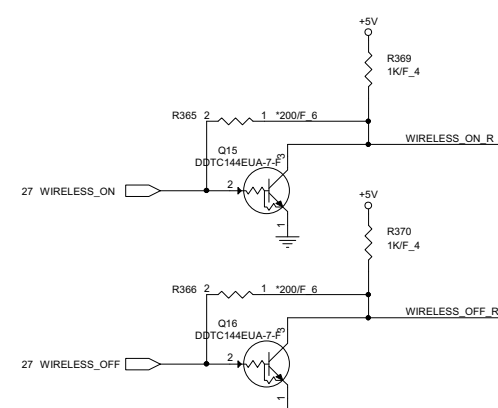


Need Change PW after DB

KEYBOARD PULL-UP

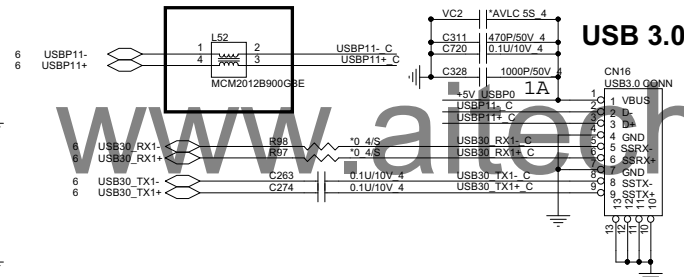
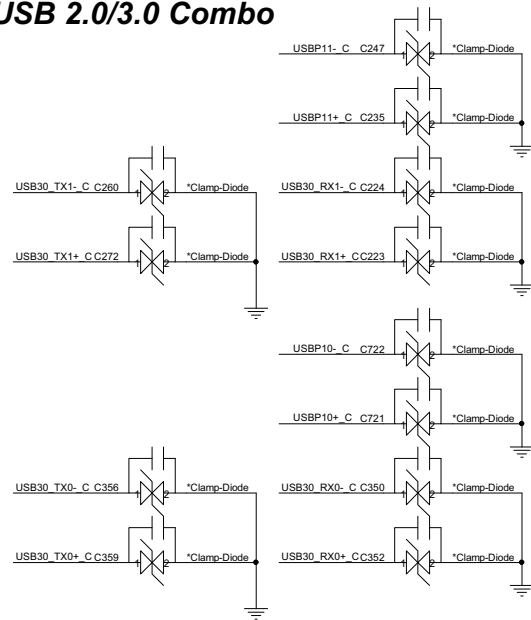


6/21/2012 for EMI



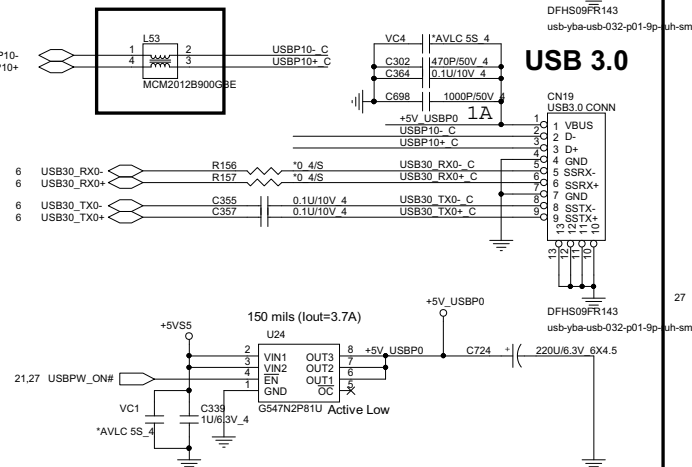
25

USB 2.0/3.0 Combo

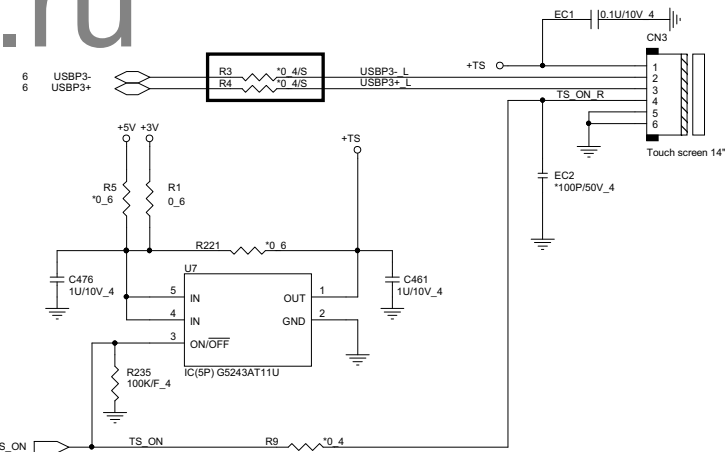


USB 3.0

USB 3.0



Touch screen

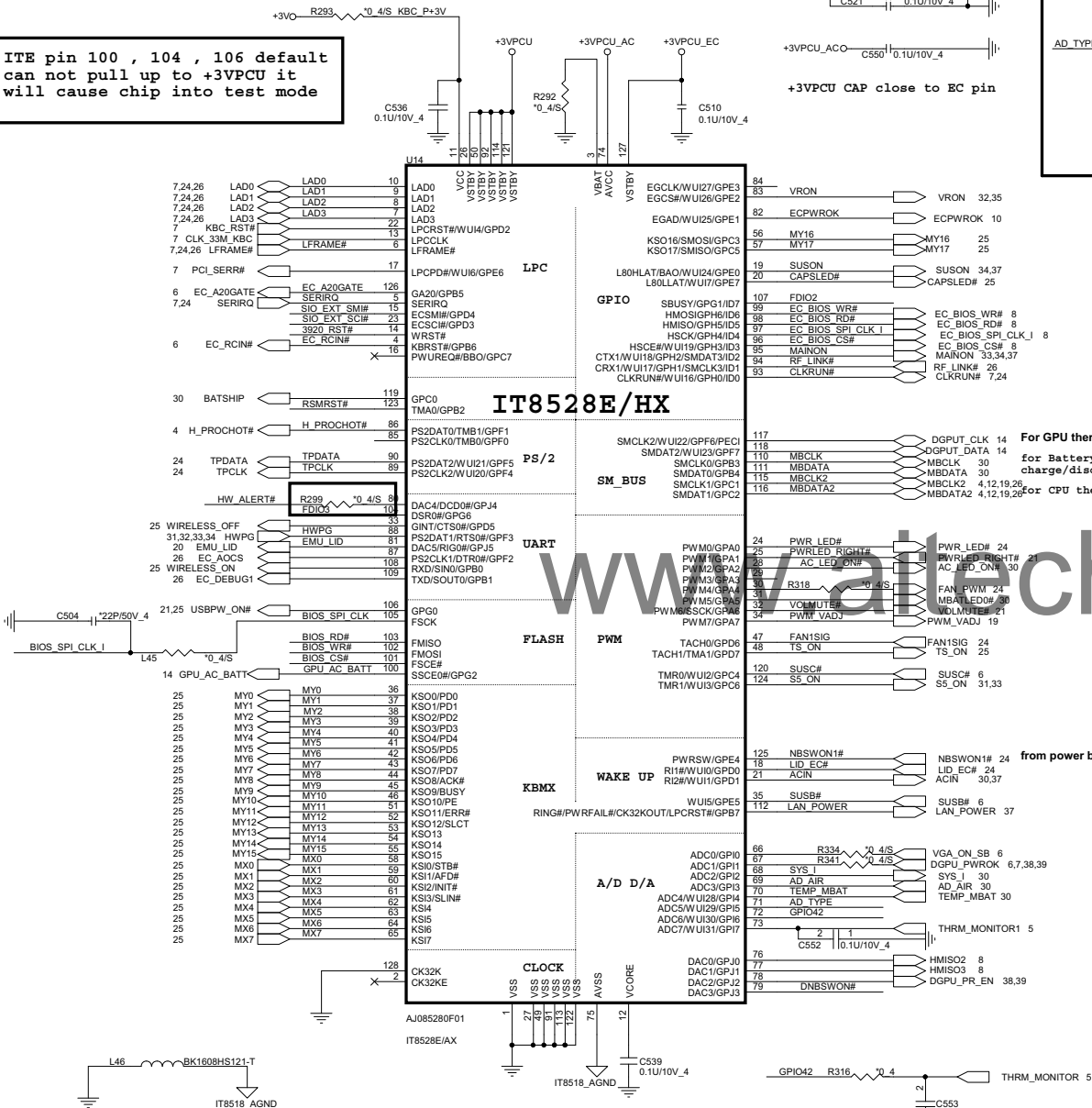


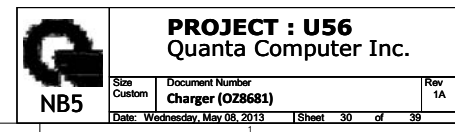
PROJECT : Richland FP2
Quanta Computer Inc.

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2,4,6,8,9,10,11,12,13,19,20,21,22,23,24,25,26,37,38,39
5,7,21,24,25,26,30,31 +3VPCU

ITE pin 100, 104, 106 default
can not pull up to +3VPCU it
will cause chip into test mode

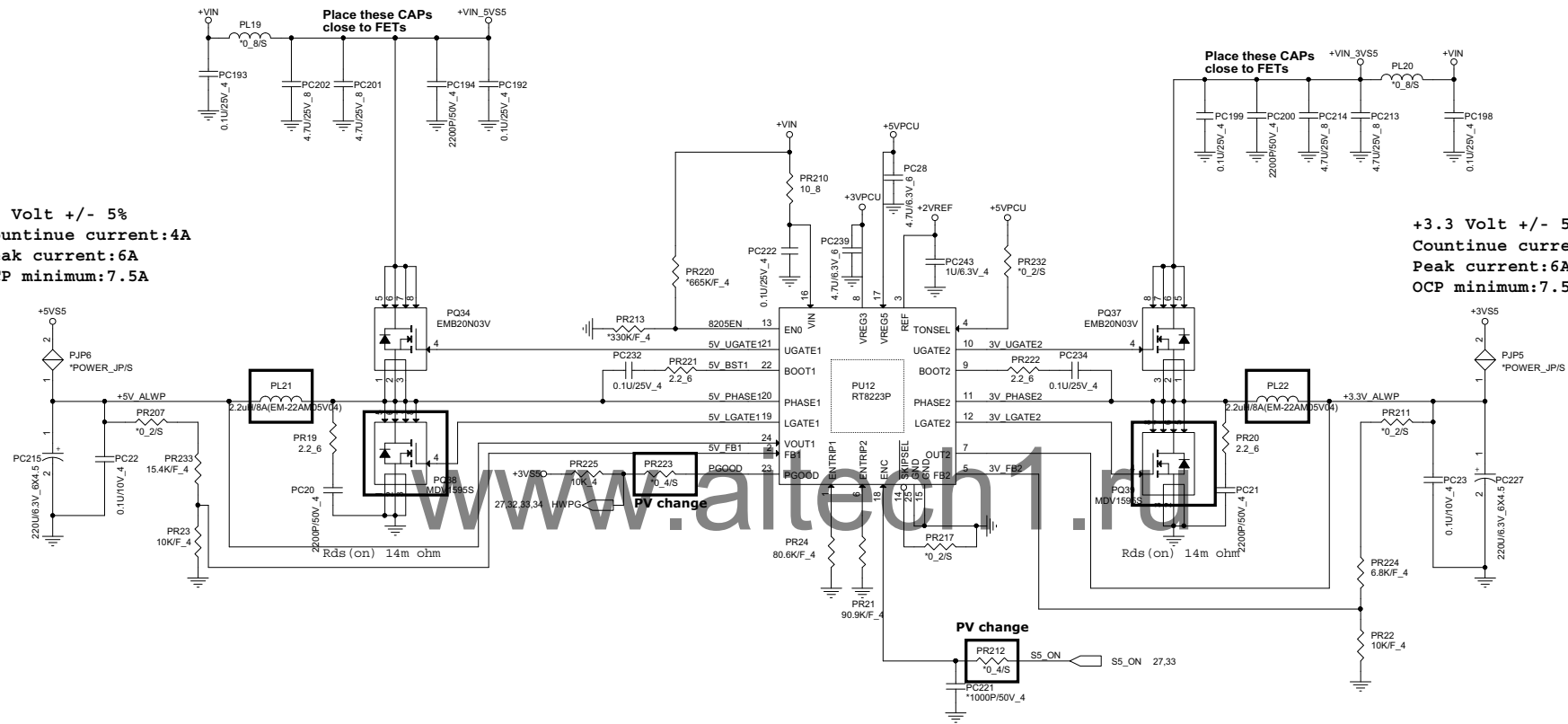




DC/DC +3VS5/+5VS5

+5 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

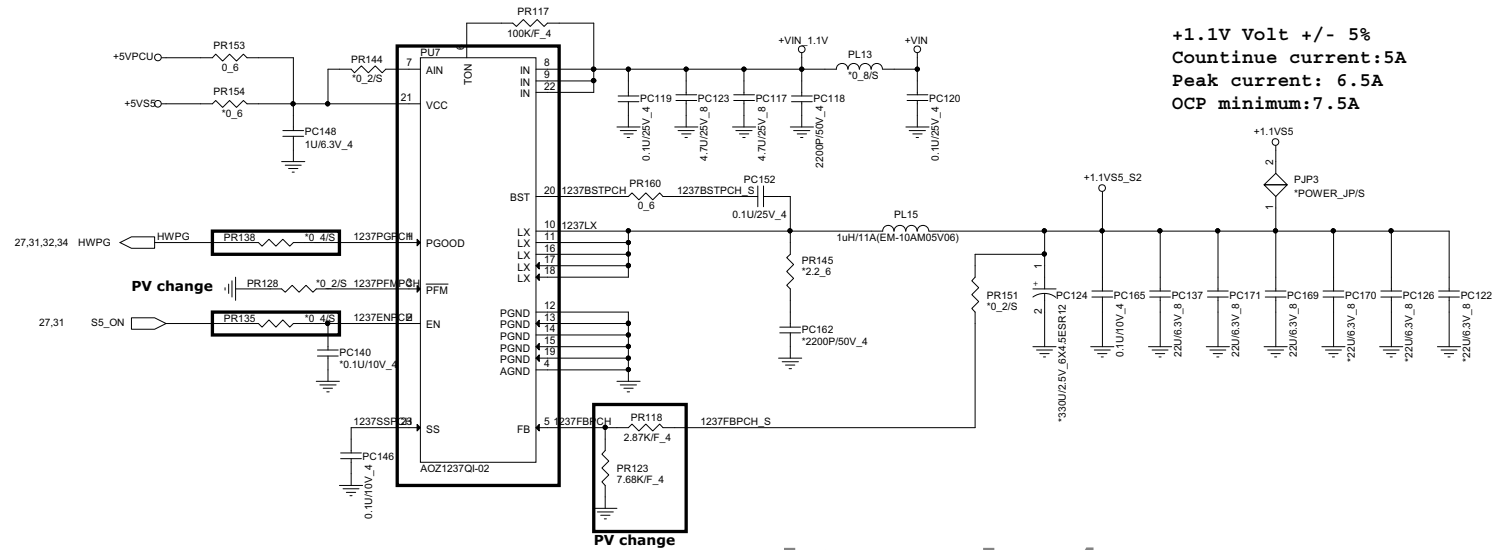


NB5

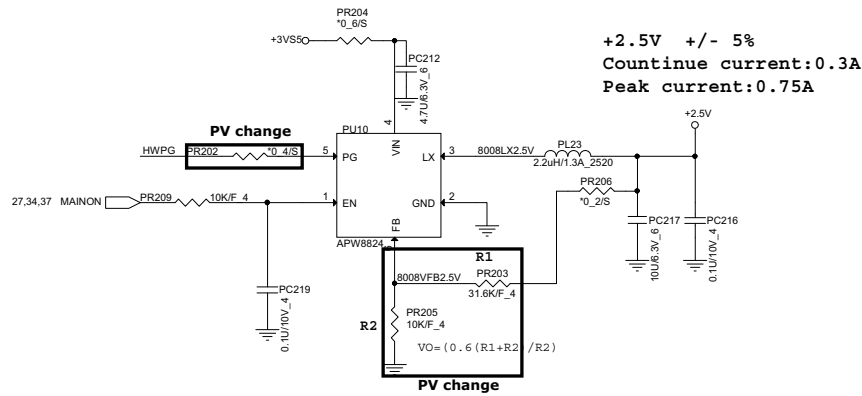
PROJECT : R33
Quanta Computer Inc.

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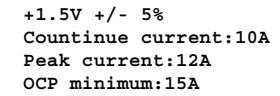


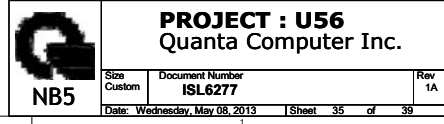
+VIN	20,24,30,31,32,34,36,37,38,39
+2.5V	5
+3VSS	6,8,9,10,26,27,31,35,37,39
+5VSS	21,25,31,32,34,35,36,37,38,39
+1.1VSS	9,37
+5VPCU	30,31

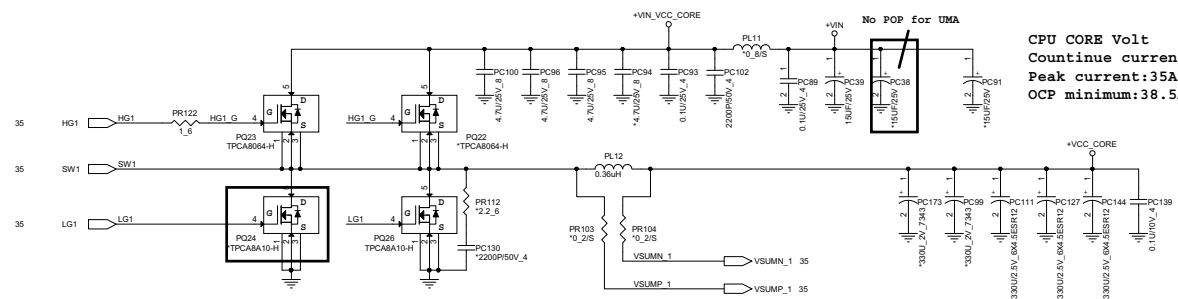


PROJECT : U56
Quanta Computer Inc.

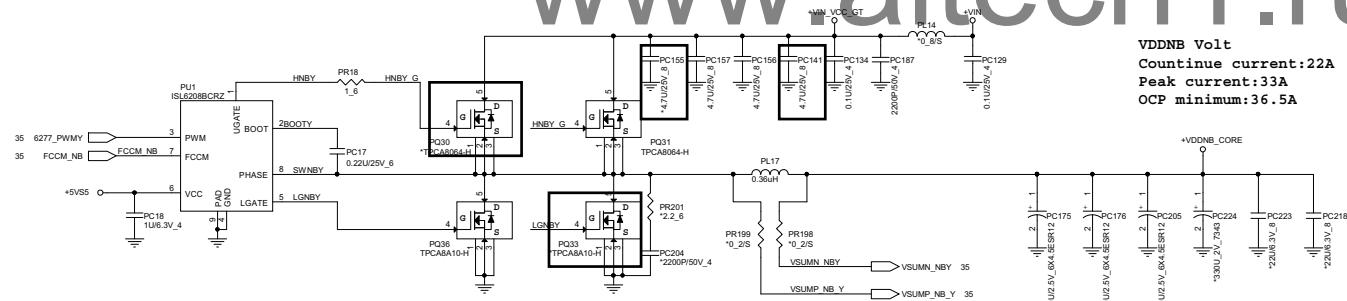
Size	Custom	Document Number	+1.1VSS (RT8228)/2.5V	Rev	1A
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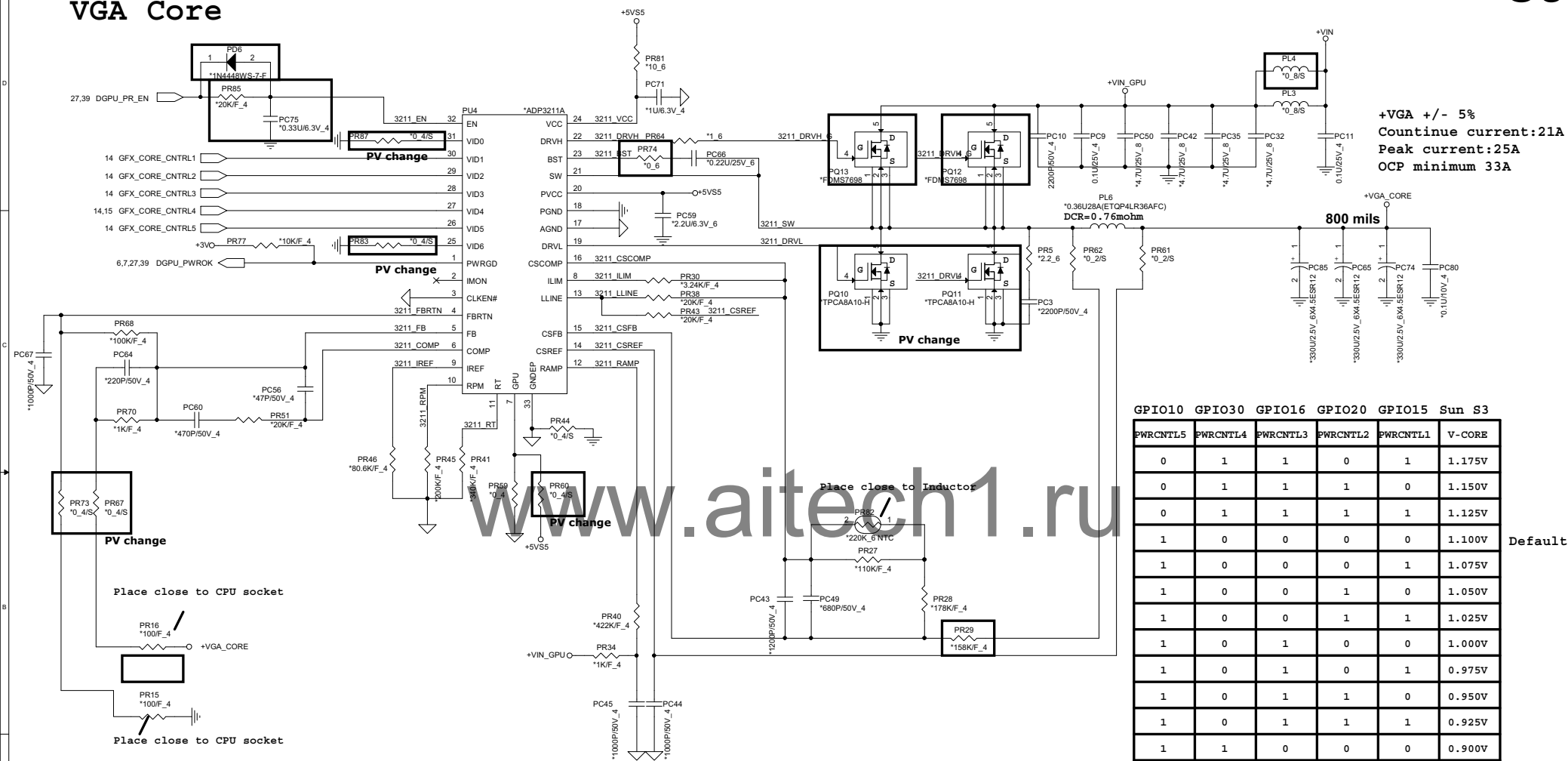
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PROJECT : U56
Quanta Computer Inc.

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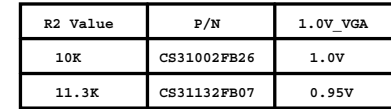
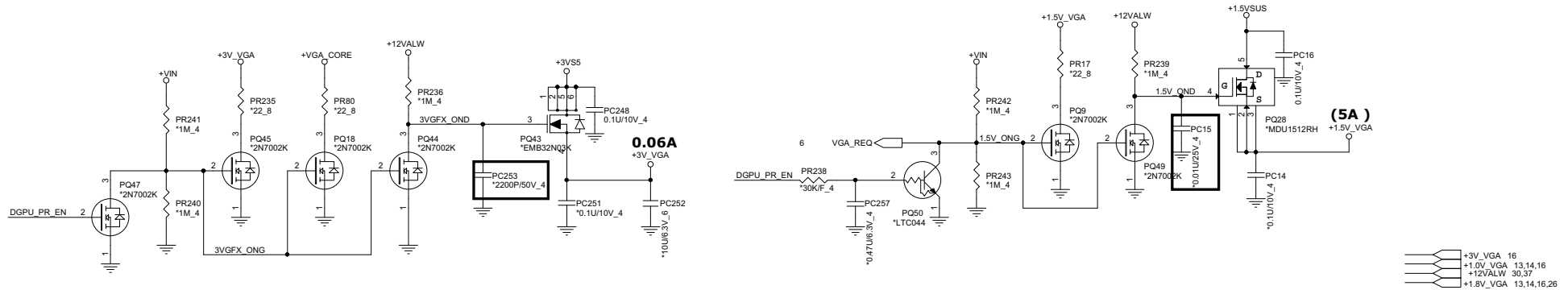
GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun S3
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default



PROJECT : U56
Quanta Computer Inc.

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[illegible]

Size Custom	Document Number +VGA POWER	Rev 1A
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